a plurality of III-nitride layers on the semiconductor substrate to provide an HEM structure; and

an internal conductor structure extending from proximate to a major surface of the HEM structure to the semiconductor substrate providing a vertical current path from the semiconductor substrate to the HEM structure, wherein the internal conductor structure comprises:

a trench;

a dielectric liner along a trench sidewall, the dielectric liner having an opening proximate to a bottom surface of the trench;

a trench filling comprising a conductive layer, wherein the trench filling makes contact to the semiconductor substrate and to a 2DEG region of the HEM device; and

a first current carrying contact adjoining a back surface of the semiconductor substrate and in electrical communication with the trench filling.

2. The semiconductor device of claim **1** further comprising an epitaxial layer between the semiconductor substrate and the plurality of III-nitride layers, wherein the epitaxial layer is of the first conductivity type and has a lower dopant concentration than the semiconductor substrate.

3. The semiconductor device of claim **1**, wherein the plurality of III-nitride layers includes a GaN channel layer and an AlGaN barrier layer on the GaN channel layer to provide the 2DEG region, and wherein the semiconductor device further comprises:

a second current carrying electrode in the AlGaN barrier layer; and

a gate structure overlying a portion of the AlGaN barrier layer and spaced apart from the second current carrying electrode, and wherein the internal connector structure forms a low resistance electrical current path from the semiconductor substrate to the AlGaN barrier layer.

4. A cascode semiconductor structure comprising:

a depletion mode HEMT device comprising:

a base substrate of a first semiconductor material, wherein the base substrate forms a first current carrying electrode;

a heterostructure comprising a III-nitride channel layer over the base substrate and a III-nitride barrier layer over the channel layer;

a second current carrying electrode coupled to the barrier layer;

a first gate electrode overlying a portion of the barrier layer and spaced apart from the second current carrying electrode; and

a first internal conductor structure extending from the barrier layer through the channel layer to the base substrate, wherein the first internal conductor structure forms a low resistance electrical current path from the base substrate to the barrier layer; and

a MOSFET device comprising:

a second gate electrode;

a third current carrying electrode electrically coupled to the first gate electrode; and

fourth current carrying electrode electrically coupled to the first internal conductor structure.

5. The structure of claim **4**, wherein the first internal conductor structure comprises:

a first conductor within the barrier layer;

a second conductor extending from the first conductor to the base substrate; and

an insulator between the second conductor layer and the channel.

6. The structure of claim **5**, wherein:

the MOSFET device comprises a separate device stacked onto the depletion mode HEMT device; and

the MOSFET device comprises a silicon substrate having opposing first and second major surfaces.

7. The structure of claim **6**, wherein:

the second gate electrode and the third current carrying electrode are disposed adjacent the first major surface of the silicon substrate;

the fourth current carrying electrode is disposed adjacent the second major surface of the silicon substrate; and

the fourth current carrying electrode is attached to the first current carrying electrode.

8. The structure of claim **7** further comprising:

a package substrate having a die pad and a plurality of leads, wherein:

the second current carrying electrode is attached to the die pad;

the first gate electrode is attached to a first lead;

the second gate electrode is electrically coupled to a second lead; and

the third current carrying electrode is electrically coupled to the first lead.

9. The structure of claim **8** further comprising:

a third lead electrically coupled to the die pad; and

an encapsulant enclosing the depletion mode HEMT device, the MOSFET device and at least portions of the first lead and at least portions of the second lead.

10. The structure of claim **6**, wherein:

the second gate electrode and the third current carrying electrode are disposed adjacent the first major surface of the silicon substrate;

the fourth current carrying electrode is disposed adjacent the second major surface of the silicon substrate; and

the fourth current carrying electrode is attached to the second current carrying electrode.

11. The structure of claim **10** further comprising:

a package substrate having a die pad and a plurality of leads, wherein:

the first current carrying electrode is attached to the die pad;

the first gate electrode is electrically coupled to a first lead;

the second gate electrode is electrically coupled to a second lead; and

the third current carrying electrode is electrically coupled to the first lead.

12. The structure of claim **11** further comprising:

a third lead electrically coupled to the die pad; and

an encapsulant enclosing the depletion mode HEMT device, the MOSFET device and at least portions of the first lead and at least portions of the second lead.

13. The structure of claim **4**, wherein the MOSFET device is disposed within the base substrate.

14. A cascode semiconductor structure comprising:

a depletion mode HEMT device comprising:

a base substrate of a first semiconductor material, wherein the base substrate forms a first current carrying electrode;

a heterostructure comprising a III-nitride channel layer over the base substrate and a III-nitride barrier layer over the channel layer;

a second current carrying electrode coupled to the barrier layer;

a first gate electrode overlying a portion of the barrier layer and spaced apart from the second current carrying electrode; and